A Systematic Study of ESD Protection Structures for RF ICs

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Abstract — **We report the first systematic investigation of various ESD protection structures, e.g., diodes, ggNMOS, gcNMOS, ggPMOS, SCR and multi-mode SCR's in a 0.35μm production BiCMOS technology, for RF ICs up to 100GHz by mixed-mode ESD simulation. Typical circuit parameters for RF ICs, e.g., parasitic resistances, capacitances, noise figures and s-parameters were studied. The comparison study suggests that compact SCR-type structures and diode strings may be solutions to RF ESD protection.**

I. INTRODUCTION

Electrostatic discharging (ESD) protection for radio frequency (RF) IC applications emerges as a major RF IC design challenge recently due to rapid increase of wireless and portable electronic devices, drawing active research efforts in the field [1-3]. Traditional ESD protection structures are generally not suitable for RF ICs. The uniqueness of RF ESD protection compared with traditional ESD protection structures lies in the complex interactions between the ESD protection units and the core IC circuit protected. These ESD-Circuit Interactions are normally not accounted for in traditional ESD protection circuit design. However, such ESD-circuit interactions may cause serious problems in chip operations [1]. On one hand, the core IC circuit may influence ESD protection operation at chip level, which is referred to as Circuit-to-ESD Influence. Typically, mis-triggering of ESD protection structures due to high-GHz RF signals may lead to short-circuit problem. On the other hand, any ESD protection structure may produce substantial parasitics, which can significantly affect the chip performance, being referred to as ESD-to-Circuit Influence. For example, parasitic resistance and capacitance associated with an ESD protection structures, i.e., R_{ESD} and C_{ESD}, may cause serious signal delay or clock corruption at chip level. In addition, these ESD-induced R_{ESD} and C_{ESD} will lead to on-chip impedance matching problem, leading in decrease in power delivery efficiency and reduction in bandwidth, etc. Particularly, variation in C_{ESD} values due to process fluctuation, biasing and temperature effect makes it extremely difficult to account for ESD protection effects in RF IC design. Another big problem is the ESD-induced noise performance deteriorations of RF and mixed-signal ICs. These include the extra noises generation by the ESD protection structures as well as significant noise coupling effects between I/O and the substrate, which causes the troublesome cross-chip noise traveling problem. Hence, the right approach in designing RF ESD protection circuits is to pursue novel compact low-parasitic ESD protection structures and to thoroughly evaluate the ESD-Circuit Interactions at full chip level, as opposed to treating ESD protection design separately from RF IC design - still a common practice currently. Recent papers report many possible RF ESD protection structures [1]. For example, using simple protection diode strings that are supposed to have linearly reduced C_{ESD} due to series capacitor connection. Other designs include multi-mode compact SCR-type (silicon controlled rectifier) ESD structures that reduce total ESD device counts, resulting in lower parasitic effects and less Si area consumption. However, there has been no systematic evaluation of commonly used traditional ESD protection structures, e.g., diodes, ggNMOS (grounded-gate NMOSFET), gcNMOS (gate-coupled NMOS), ggPMOS (PMOS with gate and source shortened to V_{DD}), SCR, dual-direction SCR (dSCR), multi-mode full-direction SCR (fSCR), etc [4], for RF ICs to justify whether one specific ESD protection structure is a suitable RF ESD protection solution quantitatively. This paper presents the first systematic study of various ESD protection structures for RF ICs in terms of RF performance merits. A mixed-mode ESD protection simulation method was used to conduct this quantitative evaluation.

II. VARIOUS ESD PROTECTION STRUCTURES

Theoretically, any I/O of an IC chip must be protected by ESD protection units against ESD stresses of different modes, i.e., I/O-to-V_{DD} positively/negatively (PD & ND modes), I/O-to-V_{SS} positively/negatively (PS & NS modes), and V_{DD}-to-V_{SS}, positively/negatively (DS & SD modes). Generally, an ESD protection device is connected between the I/O and V_{DD} / V_{SS}, where it remains in off-state in normal IC operation until an ESD transient appears that will turns on the ESD device to form a low-R (R_{on}) conducting channel to discharge ESD transients safely to avoid possible ESD damages. Most reported ESD structures are single-mode device that provides an active discharging path in one direction only [1]. Therefore, up to such traditional ESD units may be needed

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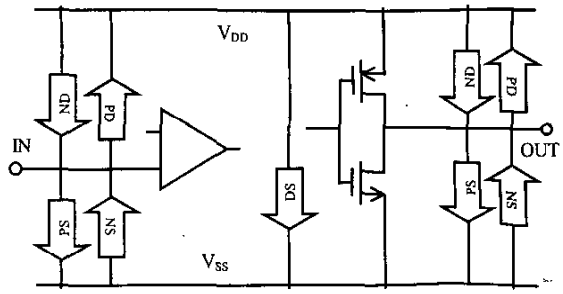

Fig. 1 A full protection scheme requires multi ESD units per I/O.

per I/O pad to realize the theoretically desired full ESD protection as illustrated in Fig. 1 for an ideal ESD protection scheme. In addition, several protection devices, called power clamps, are usually needed between power trails for power bus protection. Considering the substantial parasitics from each ESD structure, one may expect significant ESD-induced parasitic effects that will inevitably affect RF IC functionalities. Numerous working ESD protection structures exists. A diode connected in reverse mode between I/O and V_{DD} / V_{SS}, as illustrated in Fig. 2, forms the simplest ESD protection. To consider the ESD-induced parasitics, a diode ESD protection device can be readily modeled by an RC network consisting of the R_{ESD} and C_{ESD} in either parallel or series mode. The ESD-to-circuit influences can then be evaluated by replacing the protection diode by its equivalent model in simulation and analysis. A ggNMOS with its source connected to I/O and gate/drain connected to V_{SS} and a gcNMOS where a simple RC net is used to reduce the triggering voltage, shown in Fig. 2, are commonly used ESD protection units. Aiming to reduce the parasitic C_{ESD}, a diode string can be used for RF ESD protection given that the total ESD-induced parasitic C_{ESD} would be linearly reduced in the series connection format [3]. However, aspects other than the junction capacitances

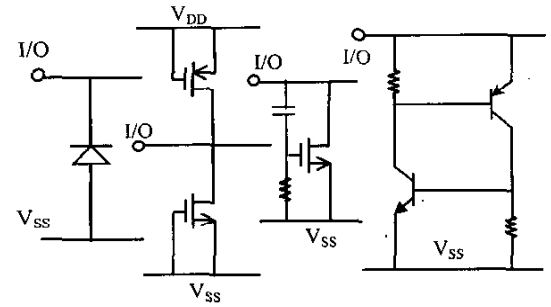

Fig. 2 Various ESD protection structures: diode, ggNMOS, ggPMOS, gcNMOS & SCR ESD protection at I/O.

must be considered as well in considering the total effects when using diode string ESD protection networks, as to be discussed later. A ggPMOS can be connected between I/O and V_{DD}, as in Fig. 2, to form a complementary full ESD protection scheme with ggNMOS. Similar R_{ESD}-C_{ESD} network may be used to evaluate the ESD-induced parasitic RC effects. A SCR structure, as shown in Fig. 2, may be a good option for RF ESD protection due to its compact size, hence, lower parasitics, given the latch-up effect may be controlled. To reduce the head counts of total ESD protection units on a chip and the overall ESD-induced parasitics, as well as Si consumption, for a full ESD protection scheme as illustrated in Fig. 1, a dual-mode SCR-type ESD structure (dSCR), shown in Fig. 3, was reported [5], which reduces total ESD unit counts per I/O pad from four (when using single-mode ESD devices such as diodes) to two, while still offering forward active ESD discharging channels between I/O and V_{DD}/V_{SS} in both directions. However, power clamping devices are still needed to protect power buses. Further, a full-mode SCR-type ESD protection (fSCR) [6] was reported for RF and mixed-signal ICs that requires only one single unit per I/O pad, which also provides an active discharging path between power tails, therefore, eliminating the need for extra power clamps. This greatly reduces the total counts of ESD units per chip, therefore, minimizing the total ESD-induced parasitic effects as well as Si consumption of ESD devices. Fig. 4 shows a typical cross-section of the fSCR structure. Noise equivalent circuit models were proposed for these ESD protection structures that can be

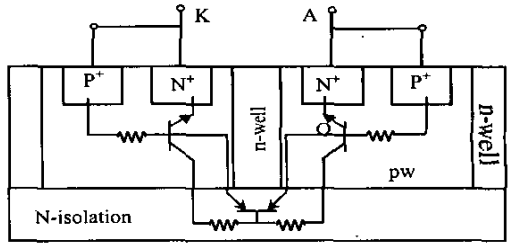

Fig. 3 X-section of dual-mode dSCR ESD protection structure.

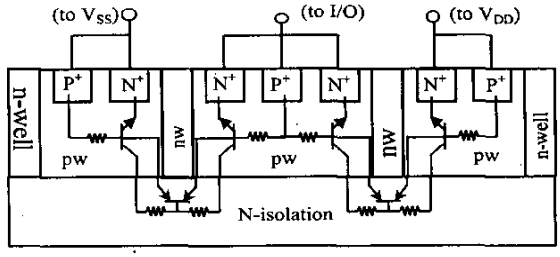

Fig. 4 X-section of full-mode fSCR ESD protection structure.

used to evaluate the noises performance [4].

III. QUANTITATIVE ANALYSIS AND DISCUSSIONS

To argue about the usefulness of various ESD protection structures to RF ICs, one ought to conduct thorough analysis of these structures in RF IC language, where suggested figures of merit include parasitic R_{ESD} & C_{ESD}, s-parameters, niose figure (NF) and Q-factors, etc [1]. We conducted a systematic study of a group of commonly used ESD structures described previously using a mixed-mode ESD protection circuit simulation method and performed detailed quantitative analysis of the results to argue the merits of these structures for RF ESD applications. These ESD devices are diode, ggNMOS, gcNMOS, ggPMOS, SCR, dSCR & fSCR. To verify the concept of using series diode strings to reduce parasitic C_{ESD}, diode strings of 2 and 5 (2xD & 5xD) diodes were also included. All these ESD structures were designed in a production 0.35μm BiCMOS technology. To justify this comparison study, the same 5kV ESD protection was targeted for all the ESD structures. Detailed mixed-mode ESD simulation was performed in designing each structure and proper device sizes were selected for layout from ESD simulation. Table I summaries the size data for these ESD structures.

Fig. 5 shows the extracted parasitic C_{ESD} values for different ESD structures. Obviously, ggNMOS, gcNMOS & ggPMOS structures produce much higher parasitic C_{ESD}. Relatively lower C_{ESD} were seen for diode with even lower C_{ESD} for the SCR as expected. The reduction in C_{ESD} in diode strings is clearly observed. In addition, it also confirms that using dual-model and full-mode dSCR and fSCR structures can substantially reduce the parasitic C_{ESD}. We should point out that the extracted C_{ESD} data are for junction capacitances only without accounting for other capacitive contributions such as metal interconnect capacitances. Head count reduction effect in using dSCR and fSCR for full ESD protection at I/O was included (marked by *). However, power-clamping devices were not considered here.

Fig. 6 shows the extracted parasitic R_{ESD} data for these ESD devices, which are supposed to be very high because ESD devices remain in off-state under normal operation. Fairly large R_{ESD} data are observed as expected. However,

Table I ESD device widths & active discharging resistances.

devices	ggNMOS	ggPMOS	Diode	2xDiode
width (um)	110	238	25	25
R_{ON} (Ω)	4.26	10.53	0.19	0.37
devices	5xDiode	SCR	dSCR	fSCR
width (um)	25	25	36	26
R_{ON} (Ω)	1.01	-	-	-

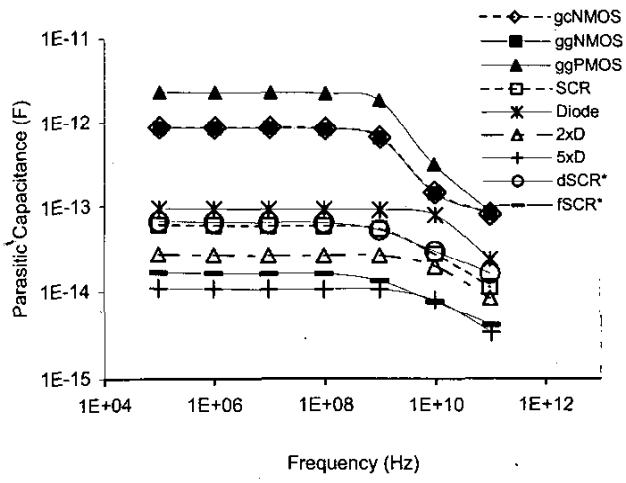

Fig. 5 Extracted parasitic C_{ESD} data for various ESD devices.

ggNMOS, gcNMOS & ggPMOS show poor R_{ESD} again. For super-GHz RF operation, the R_{ESD} drops significantly due to parasitic C_{ESD} contributions, indicating that leakage due to ESD devices may be an issue in super-GHz RF ICs.

The extracted NF data in Fig. 7 also shows poor noise performance for ggNMOS, gcNMOS & ggPMOS. Benefits of using diode strings and compact dSCR & fSCR structures are clearly shown. The NF degradation at high frequency may be contributed to noise coupling effect due to the C_{ESD}.

Figs. 8 & 9 are the extracted s-parameters for signal reflection (S11) and forward gain (S12). It is clearly observed that ggNMOS, gcNMOS & ggPMOS experience much more signal losses compared to diode and SCR type

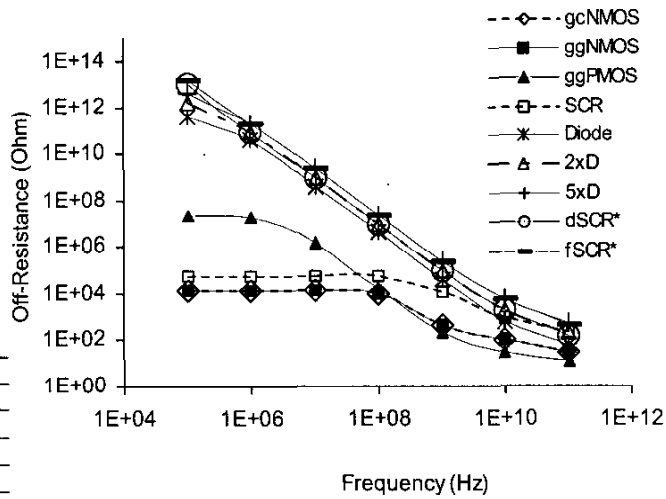

Fig. 6 Extracted parasitic R_{ESD} for various ESD devices.

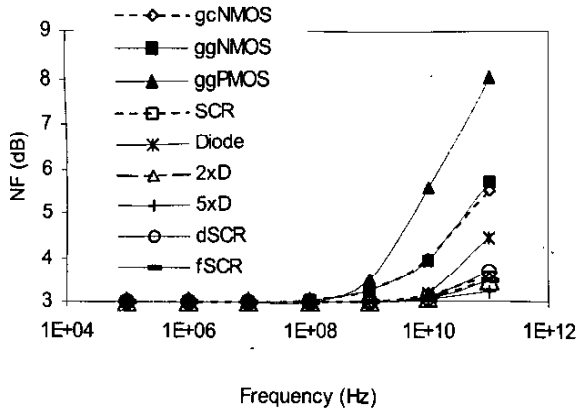

Fig. 7 Extracted NF data for various ESD devices.

ESD structures. Deterioration in signal losses at high-GHz are associated the increased C_{ESD} mismatching effects. Fig. 10 shows different layout sizes needed for various ESD devices at the same 5kV protection level. The active discharging resistances, R_{ON}, a critical parameter reflecting the ESD robustness, shown in Table I are fairly high for ggNMOS, gcNMOS & ggPMOS compared to diode networks.

In general, the results quantitatively argue that the popular MOSFET ESD devices should be avoided in RF ESD application. Diode strings seem to be a good RF ESD solution. However, several drawbacks may play a role, e.g., linearly increased layout size as shown in Fig. 10 and linearly increased R_{ON} in series. In addition, the benefit of reduced C_{ESD} may be substantially compounded when metal connect related capacitances are considered. Apparently, multi-mode SCR-type ESD structures are very attractive for RF ESD judged by all the RF parameters, as well as the layout sizes suggested in Fig. 10.

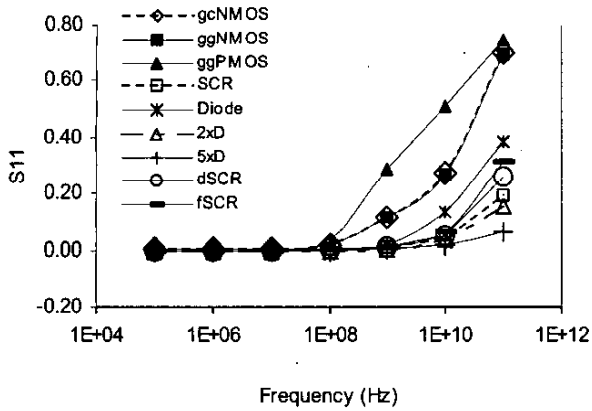

Fig. 8 Extracted S11parameters for various ESD structures.

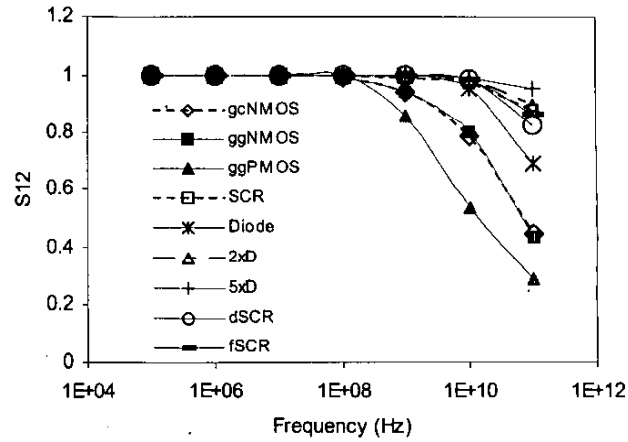

Fig. 9 Extracted S12 parameters for various ESD devices.

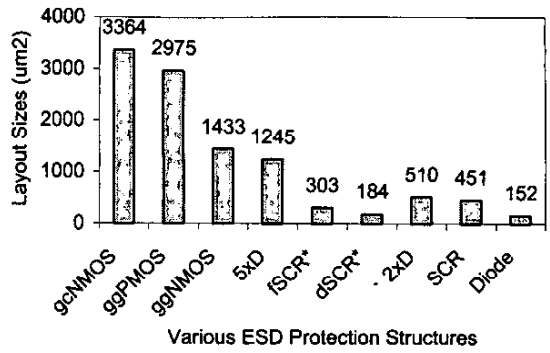

Fig 10 Different layout sizes for various ESD devices at 5kV.

V. Conclusion

In conclusion, a systematic study of commonly used ESD protection devices are conducted for RF ICs up to 100GHz. These ESD devices are designed in production 0.35um BiCMOS. Quantitative analysis shows that substantial ESD-induced parasitic effects may affect RF ICs. MOS-type ESD devices are not suitable for RF ESD. Diode strings and multi-mode SCR type ESD devices are attractive to RF ICs in terms of RF parameters and layout sizes.

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